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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/925,909 | 08/09/2001 | Takashige Ohta | 70904-56377 | 4516 |

21874 7590 05/04/2005

EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

| EXAMINER | |
|---|---|
| LIU, MING HUN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2675 | |

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/925,909 | OHTA ET AL. | |
| | Examiner | Art Unit | |
| | Ming-Hun Liu | 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7, 9-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 22-24* is/are allowed.

6)☒ Claim(s) *1-7,9 and 11-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9, 11-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese publication 10326084 to Goto Hisashi.

In reference to claim 1, Hisashi teaches a signal line drive circuit provided with a reference voltage chooser circuit (figure 2, area 38) for choosing one of incoming voltages in accordance with tones represented by an image signal to output the chosen voltage as a signal line drive signal (paragraph 14, lines 10-14), comprising a reference voltage line directly transmitting multiple first reference voltages supplied by external reference voltage (figure 1, VDD2 and ground) supply means to the reference voltage chooser circuit.

In reference to claim 2, a signal line drive circuit provided with a reference voltage chooser circuit (area 38) for choosing, in accordance with tones represented by an image signal (paragraph 10, lines 11-15), a voltage derived from multiple first reference voltages (VDD2 and ground) supplied to the signal line drive circuit from external reference voltage supply means to output a signal line drive signal. A second reference

voltage produced by voltage division (V1-V14) from at least two of the first reference voltages is supplied to the reference voltage chooser circuit via a buffer circuit (figure 1, buffers) having a high input impedance and a low output impedance; and the first reference voltages are directly (Vo and V15) supplied to the reference voltage chooser circuit in which a voltage is chosen from input voltages and then output as a signal line drive signal in accordance with the tones represented by the image signal and the first switch is controlled in accordance with the number of tones represented by the image signal (paragraph 14, lines 6-9 and paragraph 9, lines 33-34)

In reference to claims 3 and 4, Hisashi teaches a signal line drive circuit provided with a reference voltage chooser circuit (area 38) for choosing, in accordance with tones represented by an image signal (paragraph 10, lines 11-14), a voltage derived from multiple first reference voltages (VDD2 and ground) supplied to the signal line drive circuit from external reference voltage supply means to output a signal line drive signal, wherein a second reference voltage (V1-V14) produced by voltage division from at least two of the first reference voltages is supplied to the reference voltage chooser circuit via a buffer circuit (figure 1, buffer) having a high input impedance qnd a low output impedance. Hisashi also teaches that among power supply voltages supplied to the signal line drive circuit, at least a power supply voltage supplied to the buffer circuit is supplied to the buffer circuit via a first switch (SW0, SW1...SW15) controlled through a first control signal (signal from circuit 12); and the reference voltage chooser circuit chooses one of incoming voltages to output a signal line drive signal in accordance with the tones represented by the image signal.

In reference to claim 5, Hisashi teaches 5 a divider circuit for a signal line drive circuit, provided with a voltage producing a second reference voltage (V1-V14) by voltage division from at least two of first reference voltages supplied to the signal line drive circuit from external voltage supply means, the signal line drive circuit outputting a signal line drive signal in accordance with tones represented by an image signal, wherein a second switch (SW0...SW15) controlled through a second control signal (signal from circuit 12) is interposed between the first reference voltages (VDD2 and the voltage divider circuit (resistor – R in generation of V1).

In reference to claim 6, Hisashi teaches on paragraph 14, lines 6-9 and paragraph 9, lines 33-34, that the second switch is controlled in accordance with the number of tones represented by the image signal.

In reference to claim 7, Hisashi teaches a signal line drive circuit, comprising a sampling circuit for sampling an image signal so as to generate a sampling signal representative of the number of tones contained in said image signal (paragraph 14, lines 4-5). Hisashi also teaches a reference voltage chooser circuit for choosing a reference voltage in accordance with the sampling signal to output a signal line drive signal and a decoder circuit for controlling the reference voltage chooser circuit in accordance with the sampling signal (paragraph 14, lines 7-11). Hisashi also teaches that the decoder circuit is controlled through a third control signal according to a decoder table (register 35) determined by the number of tones represented by the sampling signal and the

reference voltage chooser circuit changes a reference voltage choosing pattern in response to an output of the decoder circuit (paragraph 14, lines 6-9).

In reference to claim 9, Hisashi teaches a signal line drive circuit including a sampling circuit for sampling an image signal (paragraph 14, lines 4-5), a voltage divider circuit for producing a second reference (item 2) voltage by voltage division from multiple first reference voltages (VDD2 and Ground) from external voltage supply means supplied to the signal line drive circuit, and a reference voltage chooser circuit (figure 2, voltage selection with lines 38) for choosing a voltage derived from the first reference voltages (V0 and V15) to output a signal line drive signal. Hisashi's invention also includes a second reference voltage (voltages V1-V14) being supplied to the reference voltage chooser circuit via a buffer circuit (Buffers inside circuit 2) having a high input impedance and a low output impedance. Hisashi's reference voltage chooser circuit chooses one of incoming voltages, the signal line drive circuit including a decoder circuit for controlling the reference voltage chooser circuit in accordance with the sampled signal and outputting the signal line drive signal in accordance with tones represented by the sampled signal (paragraph 14, lines 4-11). Hisashi teaches a first switch to cut off power supply to the buffer circuit, wherein at least any one of the first are controlled for closure/opening or changed in accordance with the number of tones represented by the image signal (paragraph 14, lines 6-9 and paragraph 9, lines 33-34).

In reference to claim 11, Hisashi teaches a an image display device, comprising pixels arranged in a matrix form (figure 2, pxl), signal lines connected to the pixels and

scan lines connected to the pixels (figure 2); a scan signal line drive circuit for supplying scan signals to the scan lines for a vertical scan (item 31) and a signal line drive circuit for supplying signal line drive signals to the signal lines (figure 2), the signal line drive circuit including a reference voltage chooser circuit for choosing (area 38), in accordance with tones represented by an image signal, a voltage derived from multiple incoming first reference voltages from external reference voltage supply means (VDD2 and Ground) to output the chosen voltage, a second reference voltage produced by voltage division from at least two of the first reference voltages (V1-V14) is supplied to the reference voltage chooser circuit via a buffer circuit (buffers in figure 1) having a high input impedance and a low output impedance; and the first reference voltages are directly supplied to the reference voltage chooser circuit (V0 and v15) in which a voltage is chosen from input voltage an output a signal line drive signal in accordance with the tones represented by the image signal (paragraph 14, lines 6-9 and paragraph 9, lines 33-34).

In reference to claim 12, in paragraph 5, lines 1-4, Hisashi teaches that his invention is used for a portable device.

In reference to claim 13, Hisashi teaches a an image display device, comprising pixels arranged in a matrix form (figure 2, pxl), signal lines connected to the pixels and scan lines connected to the pixels (figure 2); a scan signal line drive circuit for supplying scan signals to the scan lines for a vertical scan (item 31) and a signal line drive circuit for supplying signal line drive signals to the signal lines (figure 2), the signal line drive circuit including a reference voltage chooser circuit (area 38) for choosing, in accordance

with tones represented by an image signal, a voltage derived from multiple incoming first reference voltages (VDD2 and ground) from external reference voltage supply means to output the chosen voltage, wherein a second reference voltage (V1 – V14) produced by voltage division from at least two of the first reference voltages is supplied to the reference voltage chooser circuit via a buffer (buffers in figure 1) circuit having a high input impedance and a low output impedance. Hisashi also teaches that among power supply voltages supplied to the signal line drive circuit, at least a power supply voltage supplied to the buffer circuit is supplied to the buffer circuit via a first switch (SW1, SW2.. SW15) controlled through a first control signal (from circuit 12); and the reference voltage chooser circuit chooses one of incoming voltages to output the signal line drive signal in accordance with the tones represented by the image signal (paragraph 14, lines 6-9 and paragraph 9, lines 33-34).

In reference to claim 14, in paragraph 5, lines 1-4, Hisashi teaches that his invention is used for a portable device.

In reference to claim 15, Hisashi teaches a an image display device, comprising pixels arranged in a matrix form (figure 2, pxl), signal lines connected to the pixels and scan lines connected to the pixels (figure 2); a scan signal line drive circuit for supplying scan signals to the scan lines for a vertical scan (item 31) and a signal line drive circuit for supplying signal line drive signals to the signal lines (figure 2). Hisashi also teaches a a voltage divider circuit (figure 1, item 2) for producing a second reference voltage by voltage division from multiple first reference voltages (VDD2 and ground) from external

reference voltage supply means; and a reference voltage chooser circuit (area 38) for choosing an output in accordance with tones represented by an image signal. Hisashi also teaches a second switch (SW1) controlled through a second control signal (signal from circtui 12) is interposed between the first reference voltages (VDD2) and the voltage divider circuit (resister -R).

In reference to claim 16, in paragraph 5, lines 1-4, Hisashi teaches that his invention is used for a portable device.

Claim 17 is rejected according to the grounds presented in the rejection of claims 7 and 11.

In reference to claim 18, in paragraph 5, lines 1-4, Hisashi teaches that his invention is used for a portable device.

Claim 19 is rejected on the ground presented in the rejection of claims 7, 9 and 11.

Claim 20, Hisashi teaches in paragraph 10, lines 11-15 that the tones can be selected manually or automatically by the system, meaning that the modes can switch arbitrarily.

In reference to claim 21, in paragraph 5, lines 1-4, Hisashi teaches that his invention is used for a portable device.

***Response to Arguments***

3. Applicant's arguments with respect to claims 1-7, 9, 11-21 have been considered but are moot in view of the new ground(s) of rejection..

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,107,981 to Fujita.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ming-Hun Liu whose telephone number is (571)272-7770. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ming-Hun Liu

CHANH NGUYEN
PRIMARY EXAMINER